line 25, after "but" insert --is--, same line, after "3V," insert --and--.

Page 88, line 13, change "3.5" to --3.5V--.

IN THE CLAIMS

Please cancel Claims 1-17 without prejudice.

Please add new Claims 18-34 as follows:

--18. A multi-level non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion and having written states of first, second,...,(n-1)th and nth (n not less than 3) storage levels;

a plurality of first data storage circuits for storing first data of first and second signal levels which respectively define write voltages and non-write voltages being applied to respective of said memory cells, wherein said write voltages correspond to said first signal level and promote progress of writing of data into said respective of said memory cells and said non-write voltages correspond to said second signal level and restrain writing of data into said respective of said memory cells so as to keep the written states of said memory cells;

a plurality of second data storage circuits, each coupled to each of said first data storage circuits, for storing second data of second,third,...,(n-1)th and nth logic levels; and

a plurality of programming control circuits including said first and second data storage circuits for applying said write voltages to the memory cells corresponding to the first data storage circuits storing the first data of said first signal level, for determining actual written states of said memory cells, for modifying stored first data from said first signal level to said second signal level in the first data storage circuits storing the first data of said first signal level and corresponding to the second data storage circuits storing the second data of said ith (i=2,3,...,n-1,n) logic level and the memory cells in which successful writing of said ith (respectively, i=2,3,..., n-1,n) storage level has been determined, for maintaining said stored first data at said first signal level in the first data storage circuits storing the first data of said first signal level and corresponding to the second data storage circuits storing the second data of said ith (i=2,3,...,n-1,n) logic level and the memory cells in which it has been determined that said ith (respectively, i=2,3,..., n-1,n) storage level has not been successfully written, and for maintaining said stored first data at said second signal level in the first data storage circuits storing the first data of said second signal level.

19. The device according to Claim 18, wherein said first data stored in said first data storage circuits and said

second data stored in said second data storage circuits are initially set to initial data, and then said first data of said initial data stored in said first data storage circuits are modified.

20. The device according to Claim 19, wherein said initial data are loaded from at least one input line.

21. The device according to Claim 18, wherein actual written states of the memory cells corresponding to the first data storage circuits storing the first data of said first signal level and the second data storage circuits storing the second data of said ith (i=2,3,...,n-1,n) logic level are simultaneously determined.

22. The device according to Claim 18, wherein actual written states of the memory cells corresponding to the first data storage circuits storing the first data of said first signal level are simultaneously determined.

23. The device according to Claim 18, wherein said first data of said first signal level stored in the first data storage circuits corresponding to the second data storage circuits storing the second data of said ith (i=2,3,...,n-1,n) logic level and the memory cell in which successful writing of said ith (respectively, i=2,3,...,n-1,n) storage level has been determined are simultaneously modified to the first data of said second signal level.

24. The device according to Claim 18, wherein the first data of said first signal level stored in the first data storage circuits corresponding to the memory cells in which

successful writing has been determined are simultaneously modified to the first data of said second signal level.

25. The device according to Claim 18, further comprising a plurality of data detectors for simultaneously detecting whether or not all of said first data storage circuits store the first data of said second signal level.

26. The device according to Claim 19, wherein each of said data detectors is provided for each of said first data storage circuits.

27. The device according to Claim 25, wherein said data detectors are coupled to at least one common output line, and said data detectors output a programming completion signal on said common output line when each first data storage circuit stores the first data of said second signal level.

28. The device according to Claim 27, wherein said applying, determining and modifying are continued until said data detectors output said programming completion signal.

29. The device according to claim 18, wherein said applying, determining and modifying are continued until each memory cell is sufficiently written.

30. The device according to Claim 18, wherein said write voltages are simultaneously applied to the memory cells corresponding to the first data storage circuits storing the first data of said first signal level.

31. The device according to Claim 30, wherein said write voltages differ according to said second data stored in said second data storage circuits.